FAIRCHILD LOW POWER SOLUTION

1, HARD SWITCHING MODEL
2, QRC MODEL
3, Design tips

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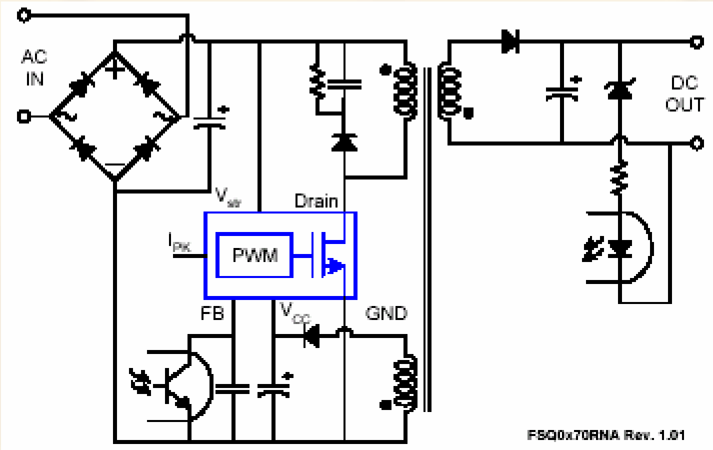
1,Fairchild power solution------APG

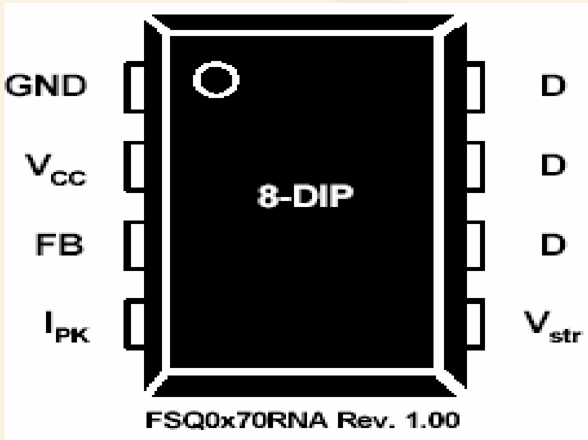
HARD SWITCHING				QRC MODEL		PWM	PFC	PWM+PFC
FSD200B	4W	FSQ211	4W	FSQ510	4W	FAN7601N	FAN7527B	ML4800
FSD210B	4W	FSQ100	7W	FSG500*	3W	FAN7601GX	FAN7528M	ML4824
FSD211H	8W	FSQ0170RNA	11W	FSQ311	8W	FAN7602N	FAN7529M	ML4803
SDM311	8W	FSQ0270RNA	13W	FSQ0165RN	11W	FAN7602M	FAN7530M	FAN4800
FSDH321	8W	FSQ0370RNA	16W	FSQ0265RN	13W	FAN7602BM		FAN4803
FSDL0165RN	11W	FSDM0465RE	40W	FSQ0365RN	16W			
FSDM0265RNB	13W	FSDM0565RE	50W					
FSDM0365RNB	16W	FSDM07652RE	60W	FSCQ0565RT	60W			
FSDM0465RB	40W			FSCQ0765RT	85W			
FSDM0565RB	50W			FSCQ0965RT	110W			
FSDM07652RB	60W			FSCQ1265RT	140W			
FSDM1265RB	90W			FSCQ1565RT	170W			
FSCM0465RG	40W							
FSCM0565RG	50W							
FSCM0765RG	60W							
FSDH0170RNB	11W							
FSDH0270RNB	13W							
FSDH0370RNB	16W							

*: under development

Green color part is we suggest part. All output power is for adapter application.

A, Hard switching model--------FSQ0170RNA





Features

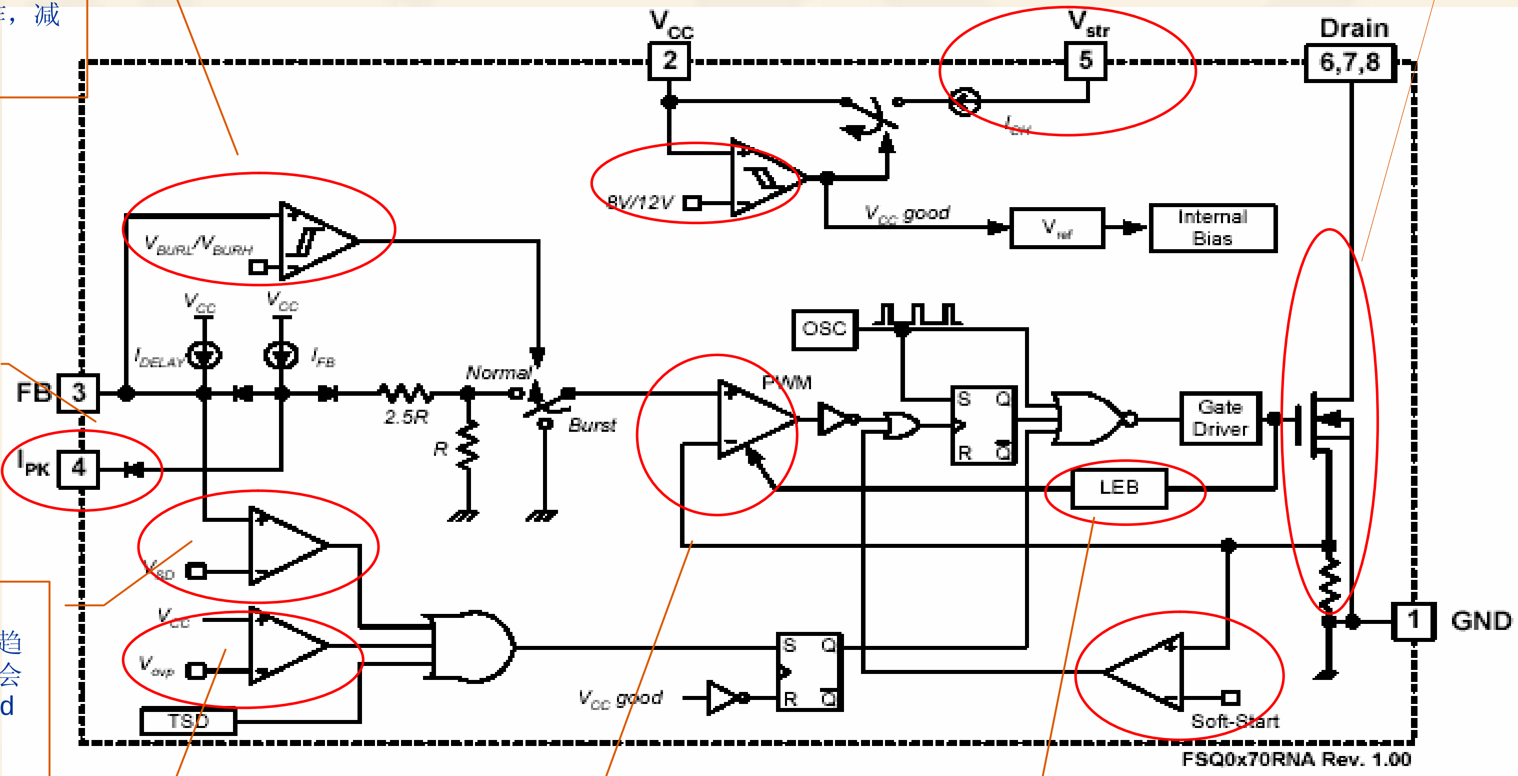
- Internal Avalanche Rugged 700V SenseFET
- Consumes only 0.8W at 230 V_{AC} & 0.5W Load with Burst-Mode Operation
- Precision Fixed Operating Frequency, 100kHz
- Internal Start-up Circuit and Built-in Soft-Start
- Pulse-by-Pulse Current Limiting and Auto-Restart Mode
- Over-Voltage Protection (OVP), Overload Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under-Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit

A, HARD SWITCHING MODEL----FSQ0170RNA

间歇工作（Burst Mode）
轻载时→输出电压上升→反馈脚的电压降低→降低到一定程度时开关停止→输出电压下降 →反馈脚上升到一定程度开关恢复
这个过程大量地减少开关动作，减小了开关损耗

高压启动开关
内部集成高压启动开关，可直接接高压，内部通过电流源向VCC电容充电，当达到启动电压后关闭，与高压断开，高压端不再提供电流，没有损耗，提高效率

内部集成增强型700V的SenseFET
（比例电流感应，省却外部电流采样电阻，极大减小功耗）



峰值电流限制调节
为逐周期过电流保护提供一个调节的机会，和过载保护高压补偿，实现高低压输出功率平衡

过载保护（OLP）
当过载时，输出电压变低，光耦趋向开路，接在反馈脚的电容电压会上升到一个较高的值，当达到Vsd时，触发OLP

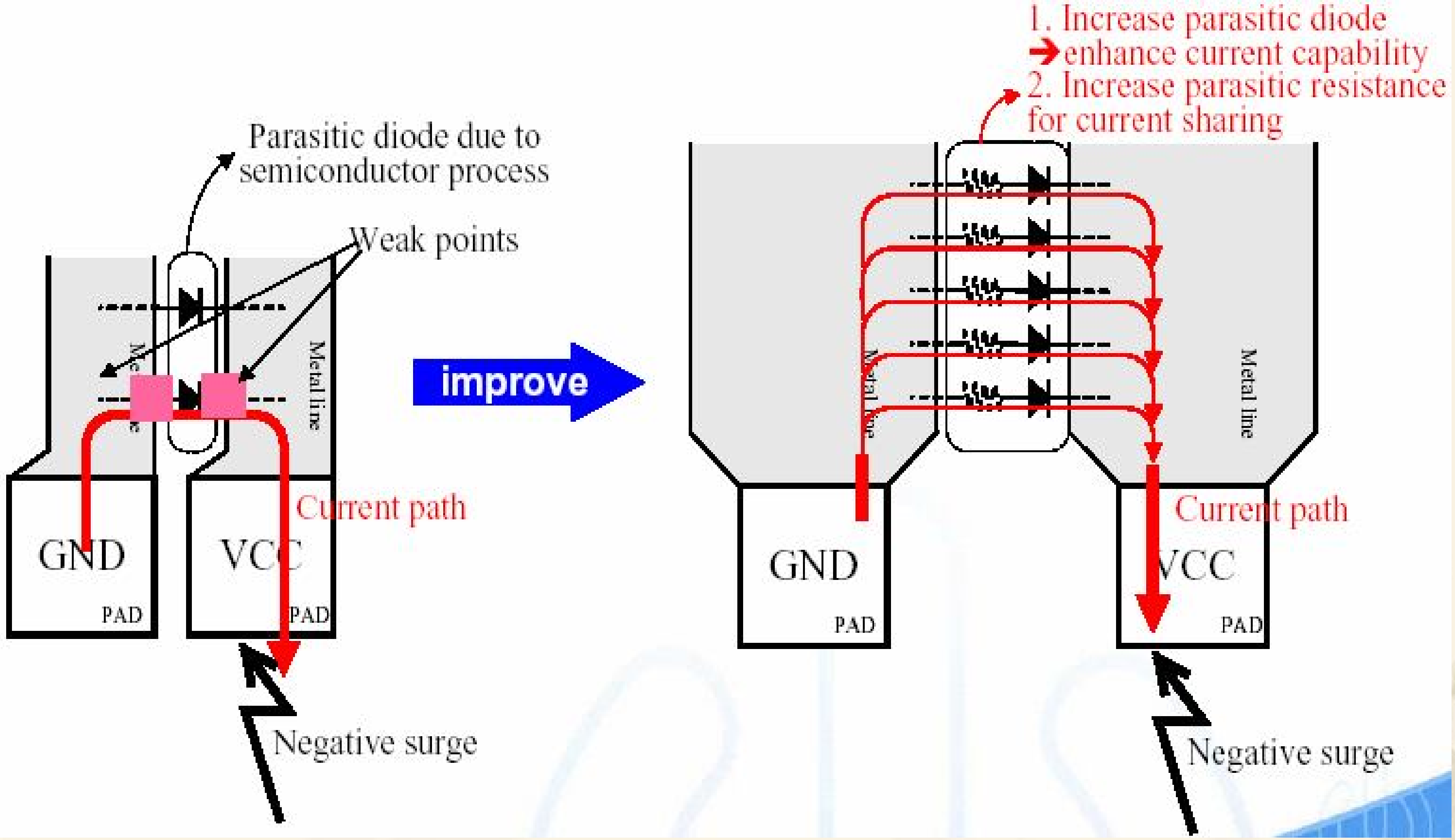
过压保护（OVP）
当反馈开路或其他原因引起VCC上升到20V时产生保护

电流模式反馈
采用电流模式反馈，具有更快的响应速度

前沿消引（LEB）
避开电流上升的前沿尖峰，消除因此引起的误动作干扰

软启动（soft start）
内部提供15mS软启动功能，减小电源启动时通过MOSFET的电流和电压应力

A,HARD SWITCHING MODEL--------FSDM0X65RE

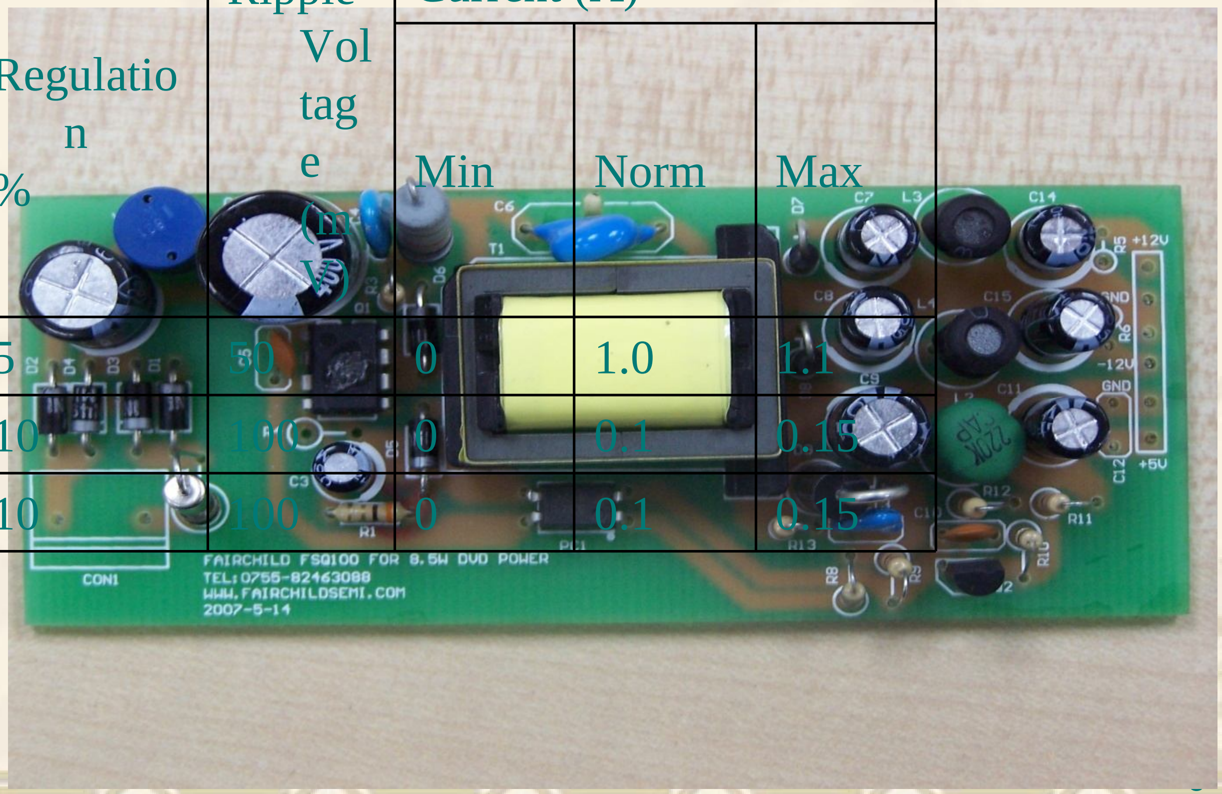


A, Design example----FSQ100 for 8W DVD power

一，Input Spec: 85Vac~264Vac

二，Output Spec:

Voltage (V)			Regulation %	Ripple Voltage (mV)	Current (A)		
Min	Nom	Max			Min	Norm	Max
4.75	5	5.25	5	50	0	1.0	1.1
10.8	12	13.2	10	100	0	0.1	0.15
-13.2	-12	-10.8	10	100	0	0.1	0.15

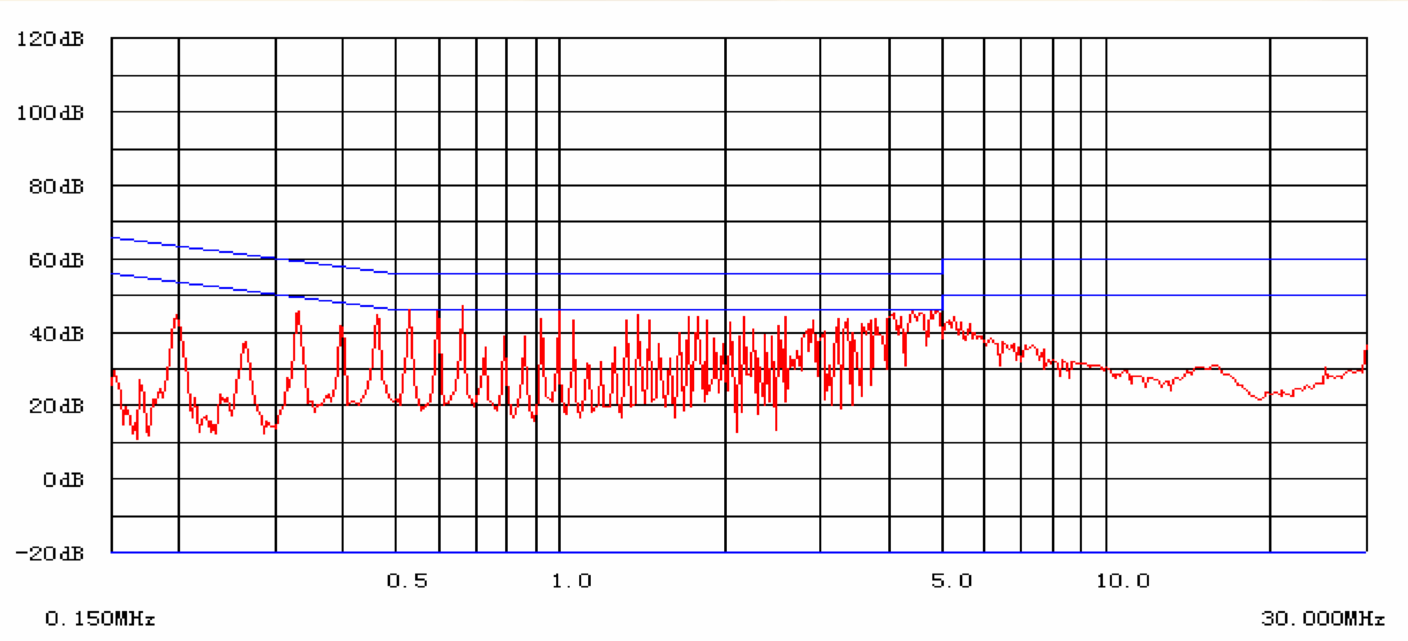


A, Design example----FSQ100 for 8W DVD power

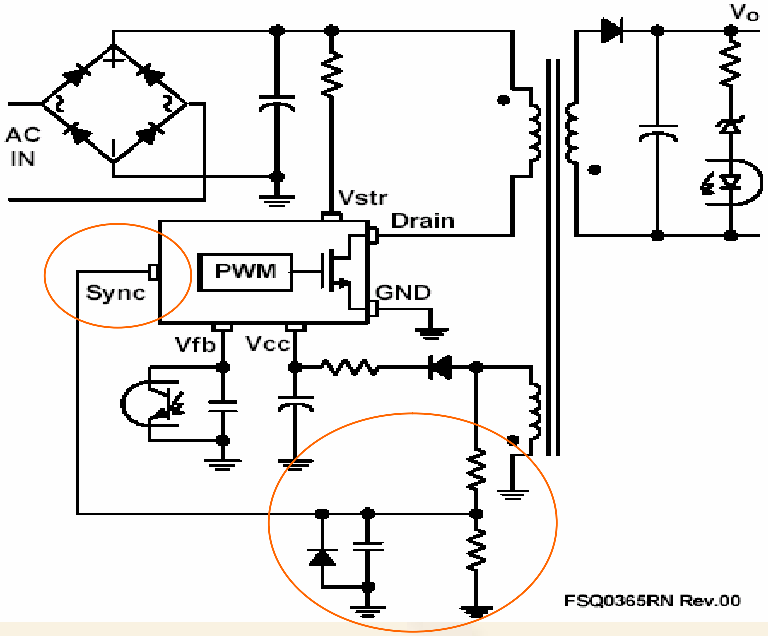
Efficiency test result

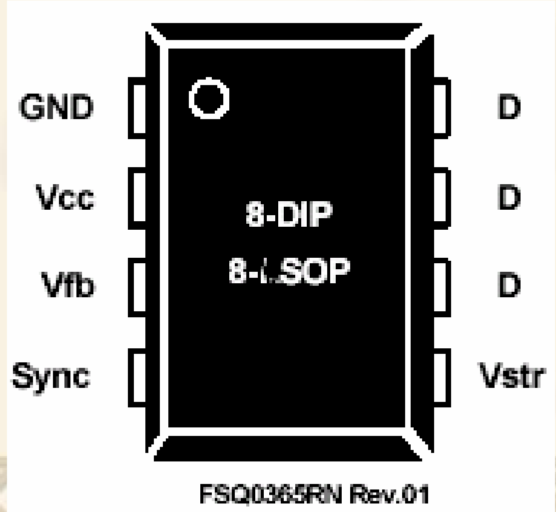
Vin (V)	Pin (W)	Pout (W)	Efficiency (%)
90	7.67	10.76	71.28
115	7.67	10.44	73.47
230	7.67	10.16	75.49
264	7.67	10.46	73.33

EMI test result



B, QRC model-------FSQ311





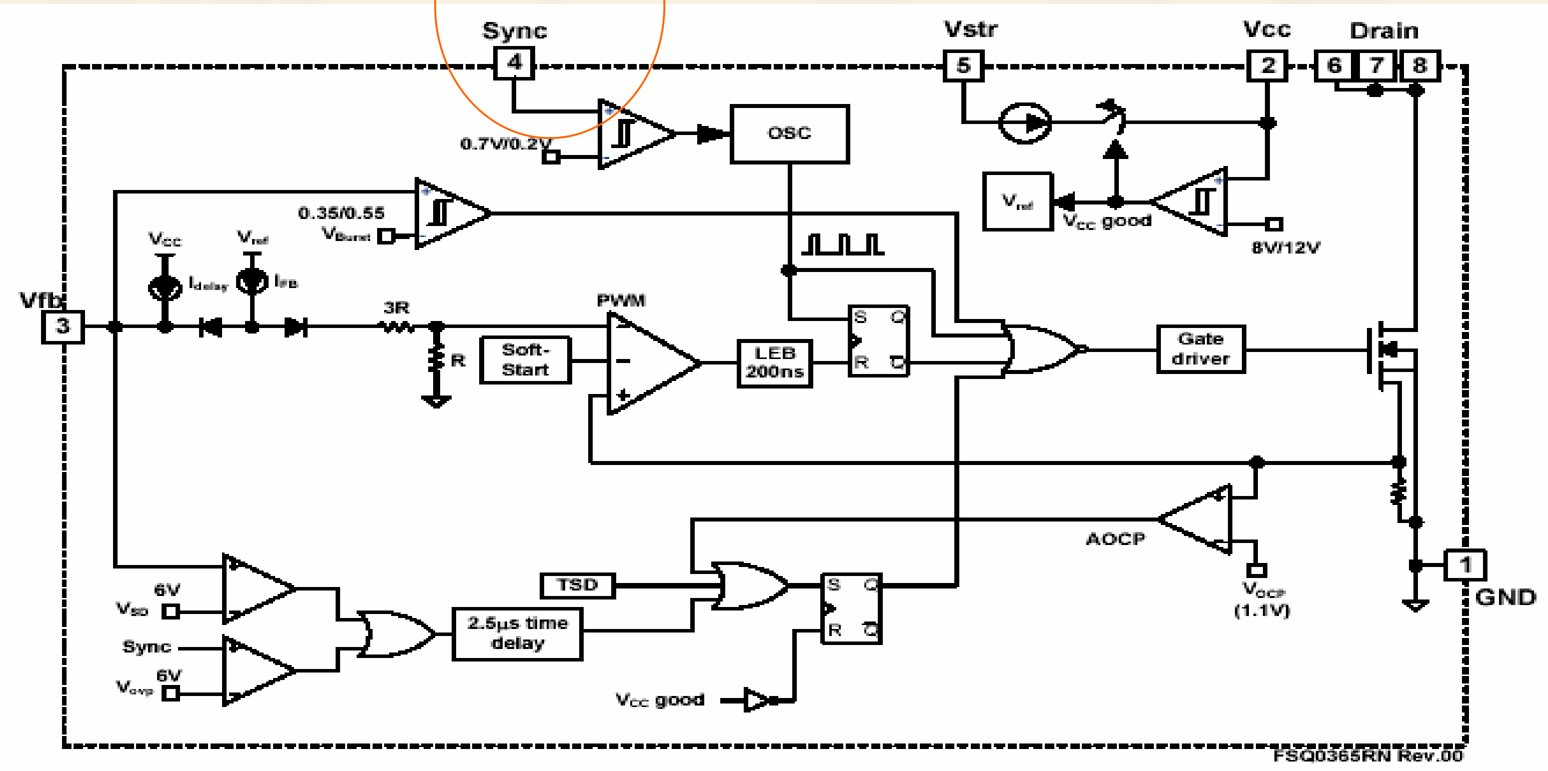
Features

- Optimized for Quasi-Resonant Converter (QRC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High-Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Start-up Circuit
- Internal High-Voltage SenseFET (650V)
- Built-in Soft-Start (15ms)

B, QRC model------FSQ311

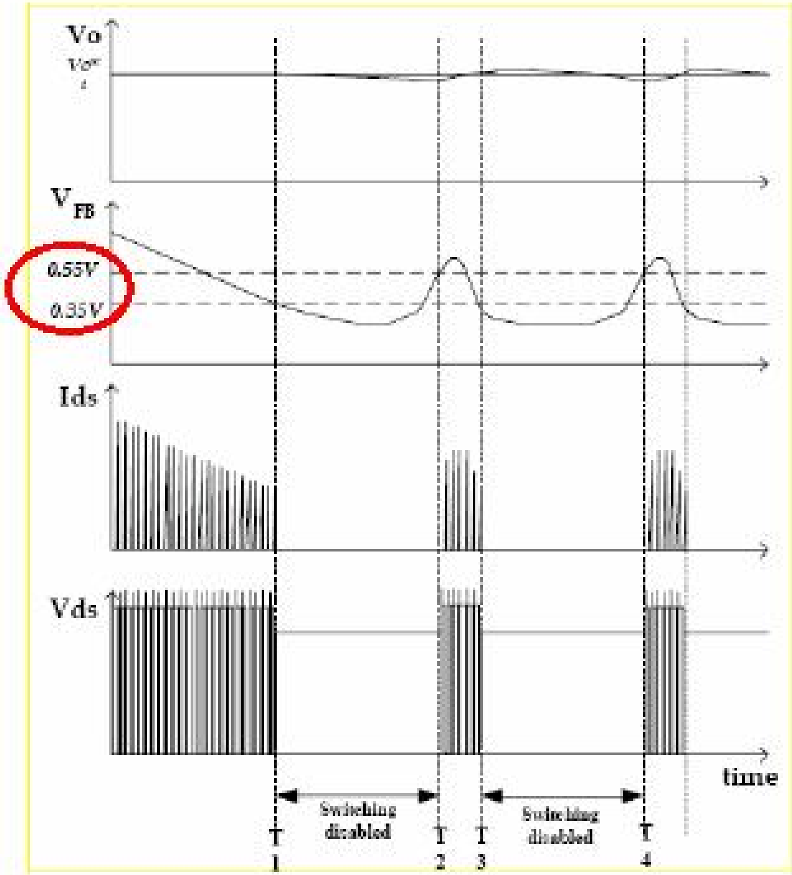
Difference:
PIN4:Sync/Ipeak

Sync OVP/ Vcc OVP



B, Burst model-------reduce standby power

- ***"Advanced Burst Mode" enables to minimize the switching loss and audible noise as well***

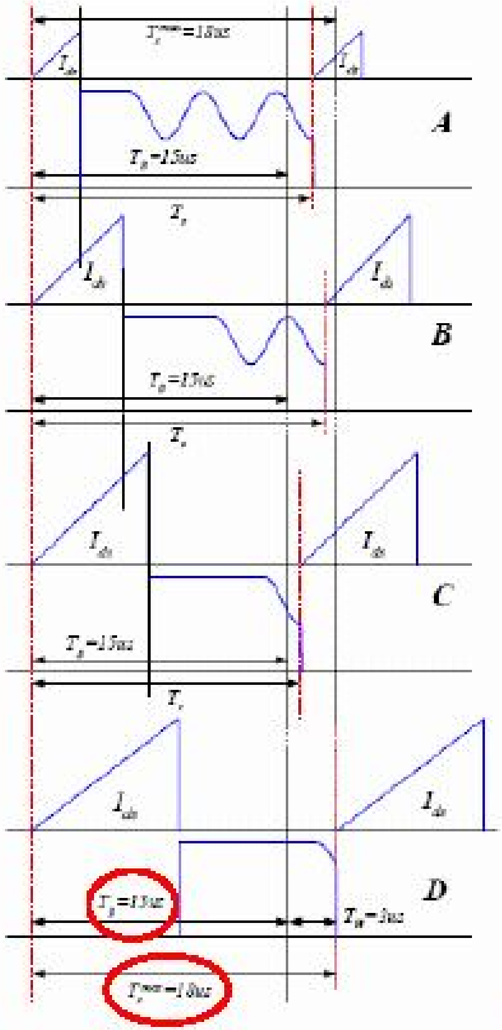


[Unit : W]

	Pin_{MAX} of FSQ0365RN			
	85Vac	110Vac	220Vac	265Vac
No Load	0.0868	0.0878	0.0998	0.1113
Pout = 0.2W	0.476	0.483	0.500	0.499
Pout = 0.5W	0.921	0.929	0.954	0.983

B, Efficiency performance

- *"Advanced Soft Switching Technology" enables to reduce switching loss*



$$T_r = 2\pi\sqrt{L_m C_{oss}} = 2\mu\,\text{sec}$$

$$\Rightarrow L_m = 1.4mH,\ C_{oss} = 73\,pF$$

Hard switching :

$$P_{turn-on\_loss} = \frac{1}{2}\cdot C_{oss}\cdot V_{ds}^2\cdot f_s$$

$$= \frac{1}{2}\cdot 73\,pF\cdot 450^2\cdot 66kHz = 488mW$$

Assume fs is same, but fs decreases in QR switching

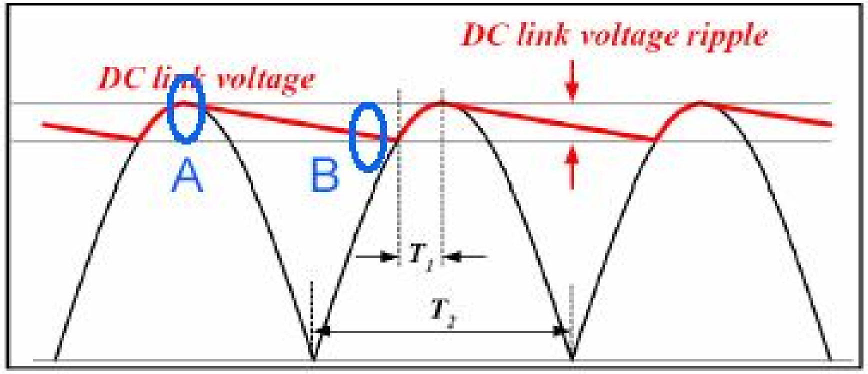
QR switching :

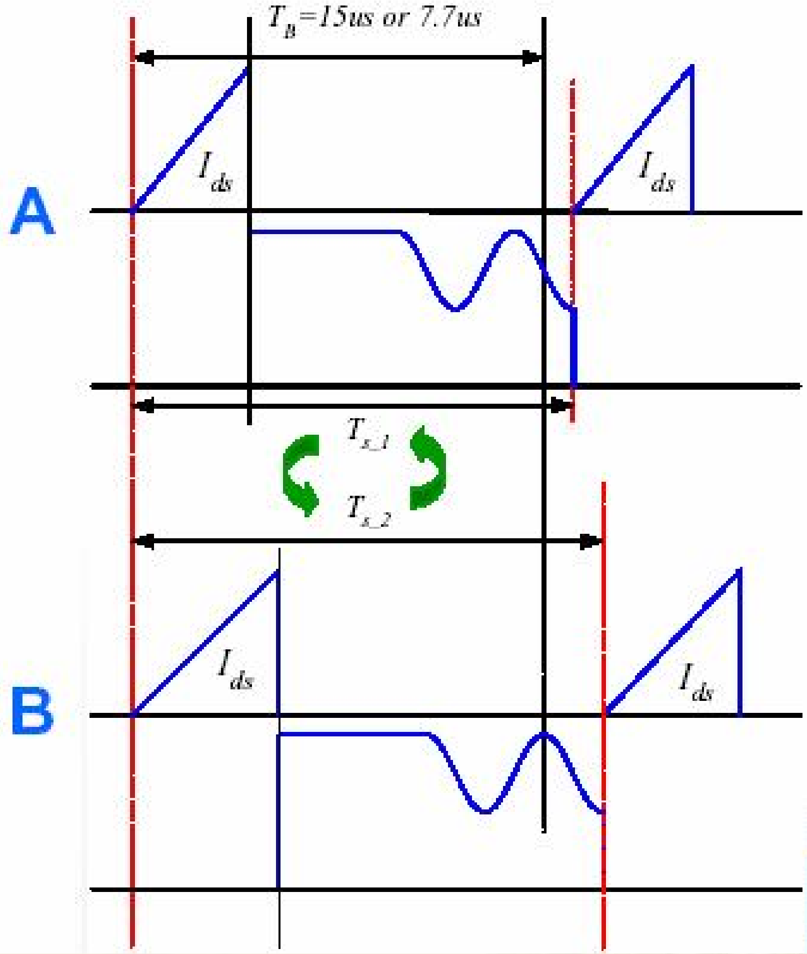
$$P_{turn-on\_loss} = \frac{1}{2}\cdot C_{oss}\cdot V_{ds}^2\cdot f_s$$

$$= \frac{1}{2}\cdot 73\,pF\cdot 300^2\cdot 66kHz = 217mW$$

B, Inherent frequency modulation

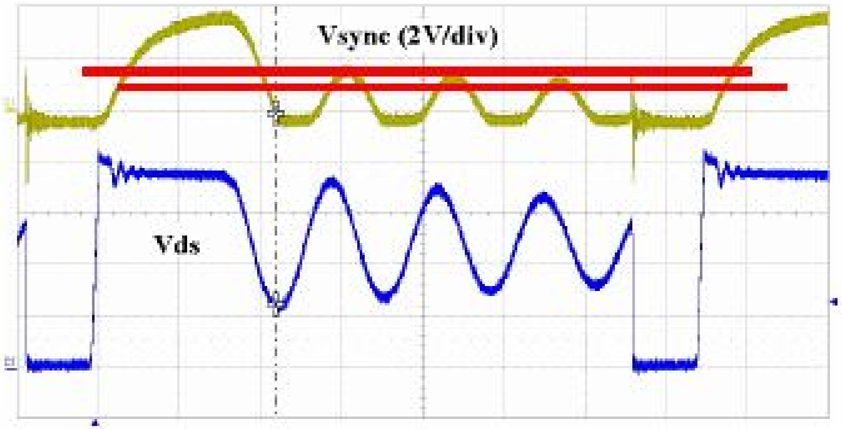
- Switching frequency is inherently modulated by the 120Hz ripple on the input voltage

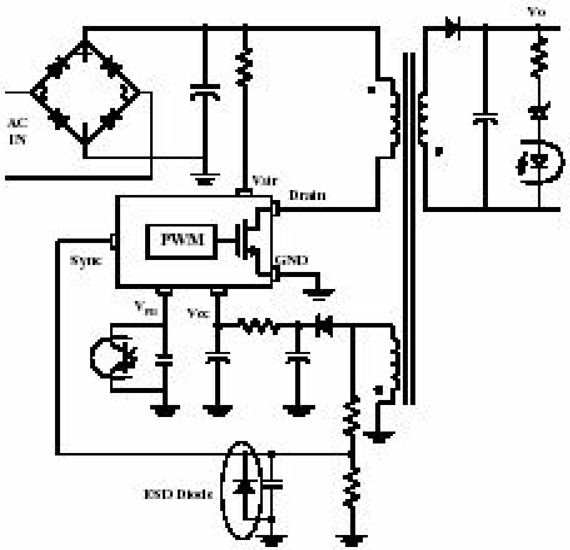


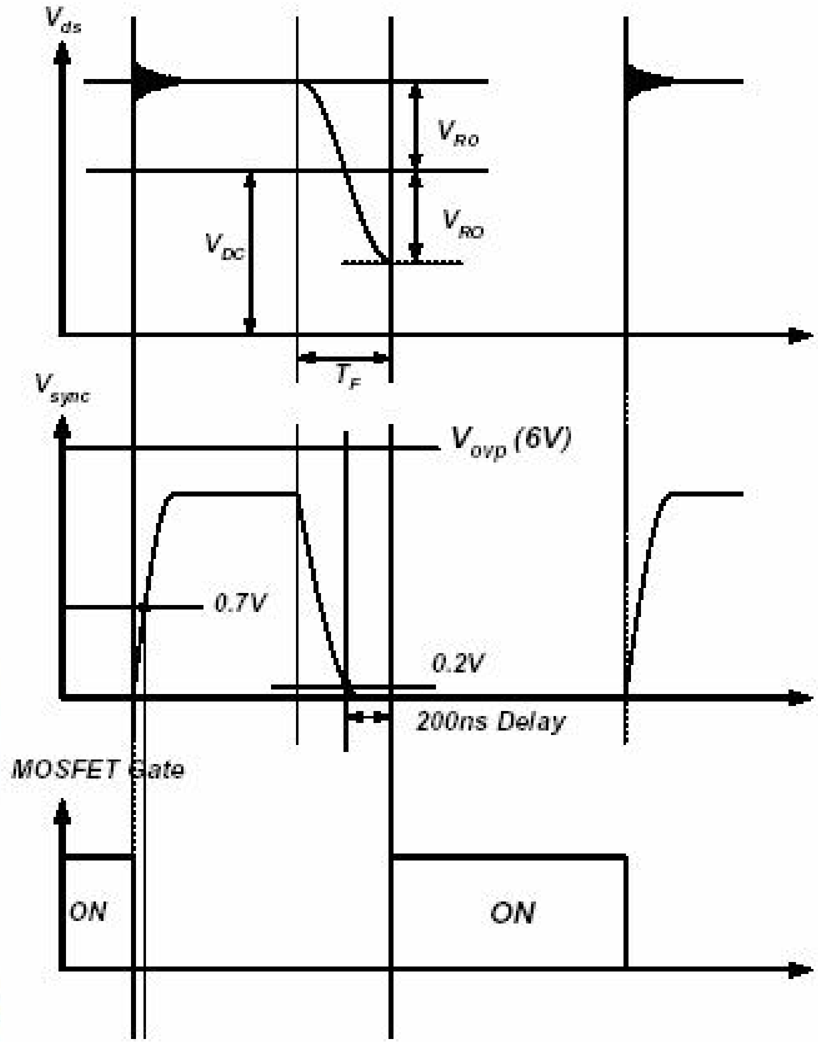


B, sync detection

- Sync voltage Threshold : 0.7V/0.2V with 200ns delay
- OVP is also detected using sync voltage (V_{ovp}=6V with 2.5us time window)







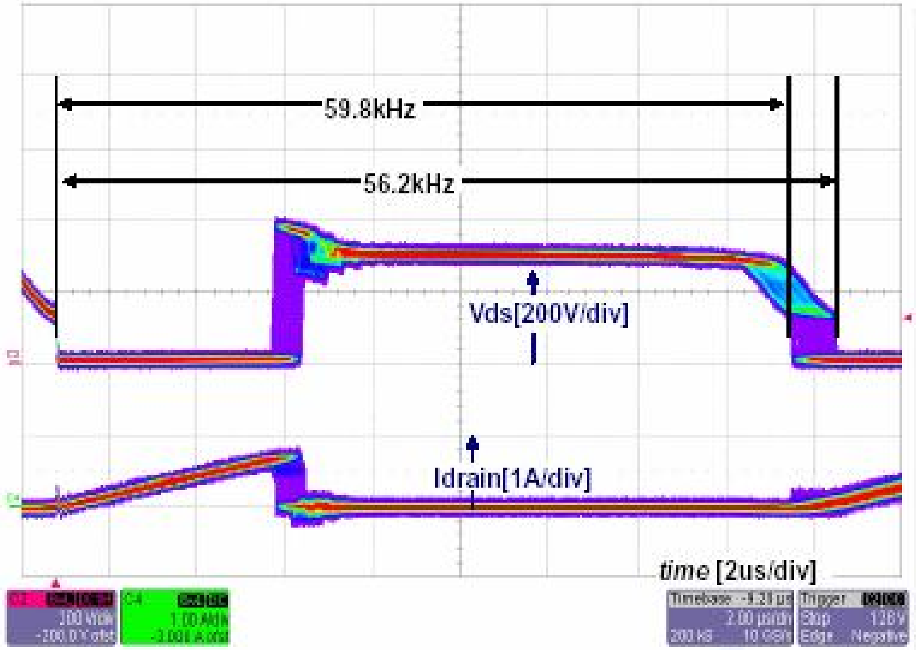
B, Design example----FSQ0365RN for 18W DVD power

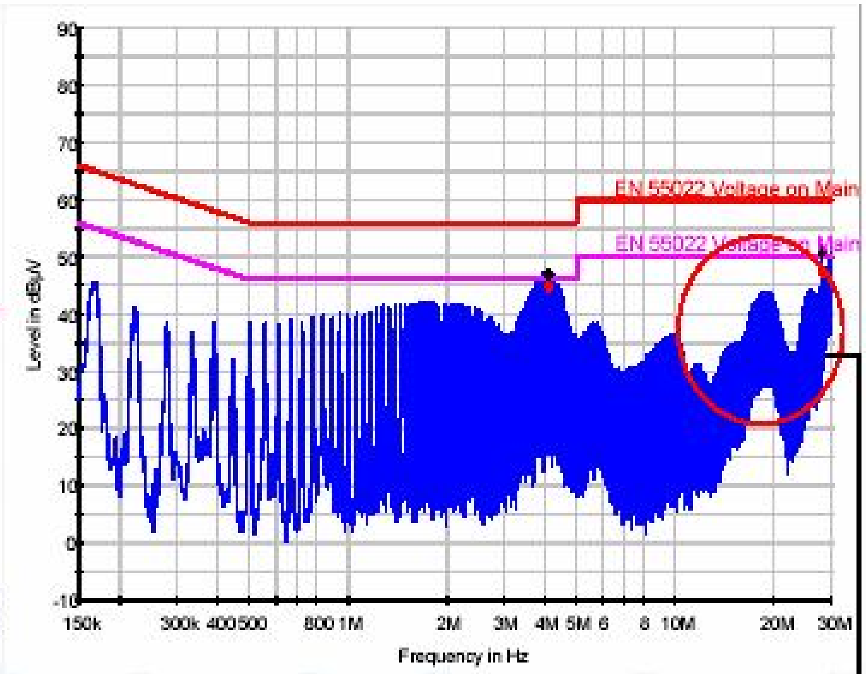
Power Supply Specification Table

Description	Min	Typ	Max	Units
Input Voltage (V_{IN})	85	-	265	V_{AC}
Output Voltage (V_{OUT1})	-	5.1	-	V_{DC}
Output Current (I_{OUT1})	-	-	1	A_{DC}
Output Voltage (V_{OUT2})	-	3.4	-	V_{DC}
Output Current (I_{OUT2})	-	-	1	A_{DC}
Output Voltage (V_{OUT3})	-	12	-	V_{DC}
Output Current (I_{OUT3})	-	-	0.4	A_{DC}
Output Voltage (V_{OUT4})	-	16	-	V_{DC}
Output Current (I_{OUT4})	-	-	0.3	A_{DC}

B, Design example----FSQ0365RN for 18W DVD power

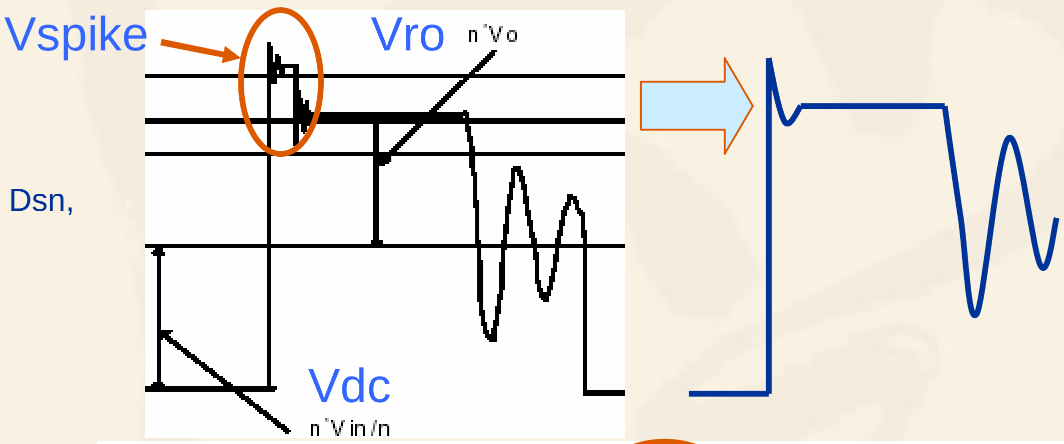
- ***By Inherent Frequency Modulation and Valley Switching, EMI noise decreases (@110Vac)***





Nearly 10dB is decreased over than 20MHz noise in case of FSQ0365

C，开关电源设计的一些考虑¡ Vds,Id,Vcc



1.控制 Vds

减小圈数比n

减小Vspike

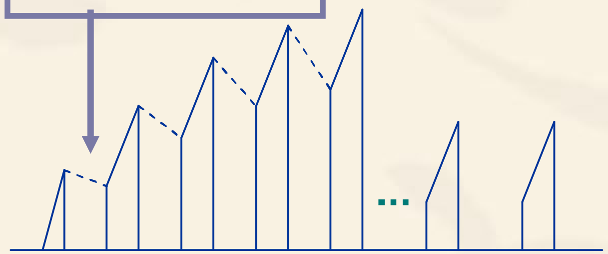
-适当选择RC,减小漏感,选用较慢速的 Dsn,

-与Dsn串联电阻

Vds=Vdc+Vro+Vspike

=Vdc+N*Vo+Vspike

di/dt=N*Vo/L



2.控制 Id

选用更大的磁心(减小饱和的可能)

增大Np

增大感量L,但太大容易饱和

增大圈数比N

$$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2P_{in}f_sK_{RF}}$$

$$N_P^{min} = \frac{L_m I_{over}}{B_{sat}A_e} \times 10^6 \quad (turns)$$

3.稳定VCC

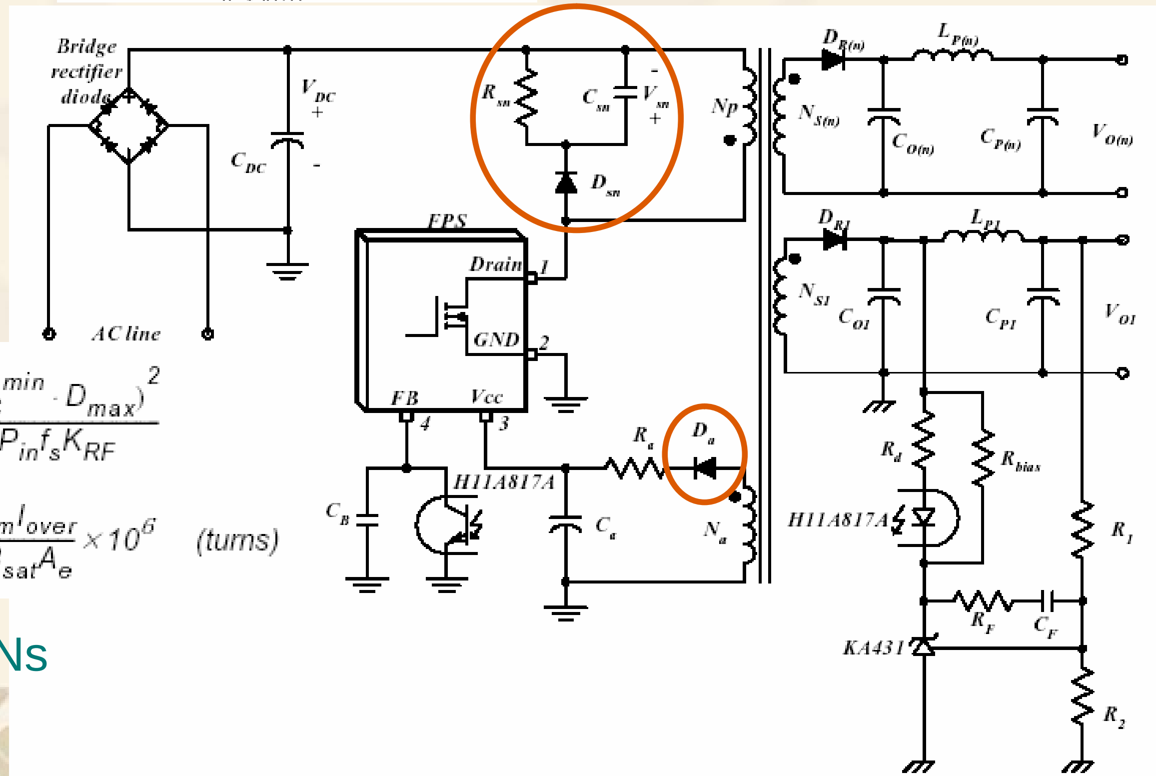
Vcc绕组位置

减小漏感

选用慢速Vcc整流二极管(Da)

适当选用Vcc限流电阻

N=Np/Ns



C,开关电源设计的一些考虑--PCB layout

1.尖端放电

在EMI电感,Y电容,L与N线之间下面尽可能放尖峰放电裸铜,给静电或其它高尖峰电压提供放电回路

2.大电流环路

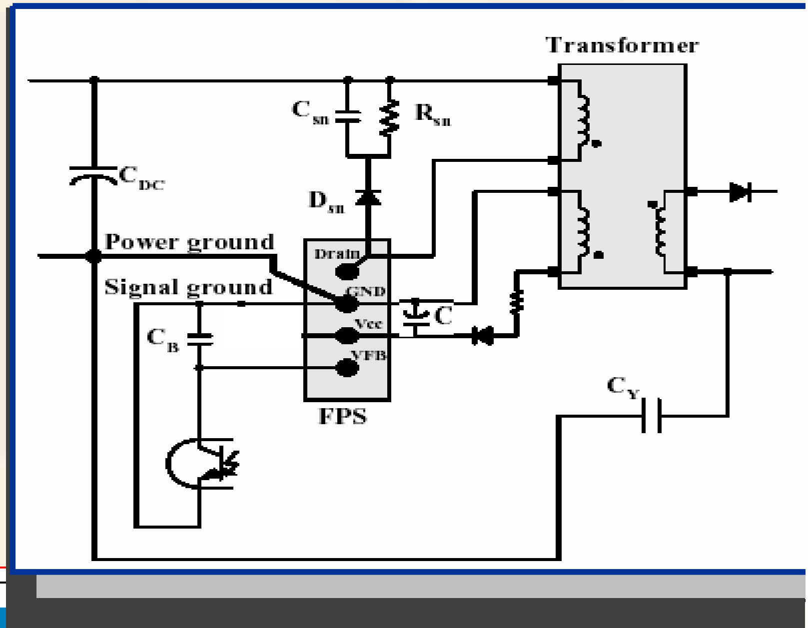
尽可能使大电流环路包围的面积最小,走线要宽

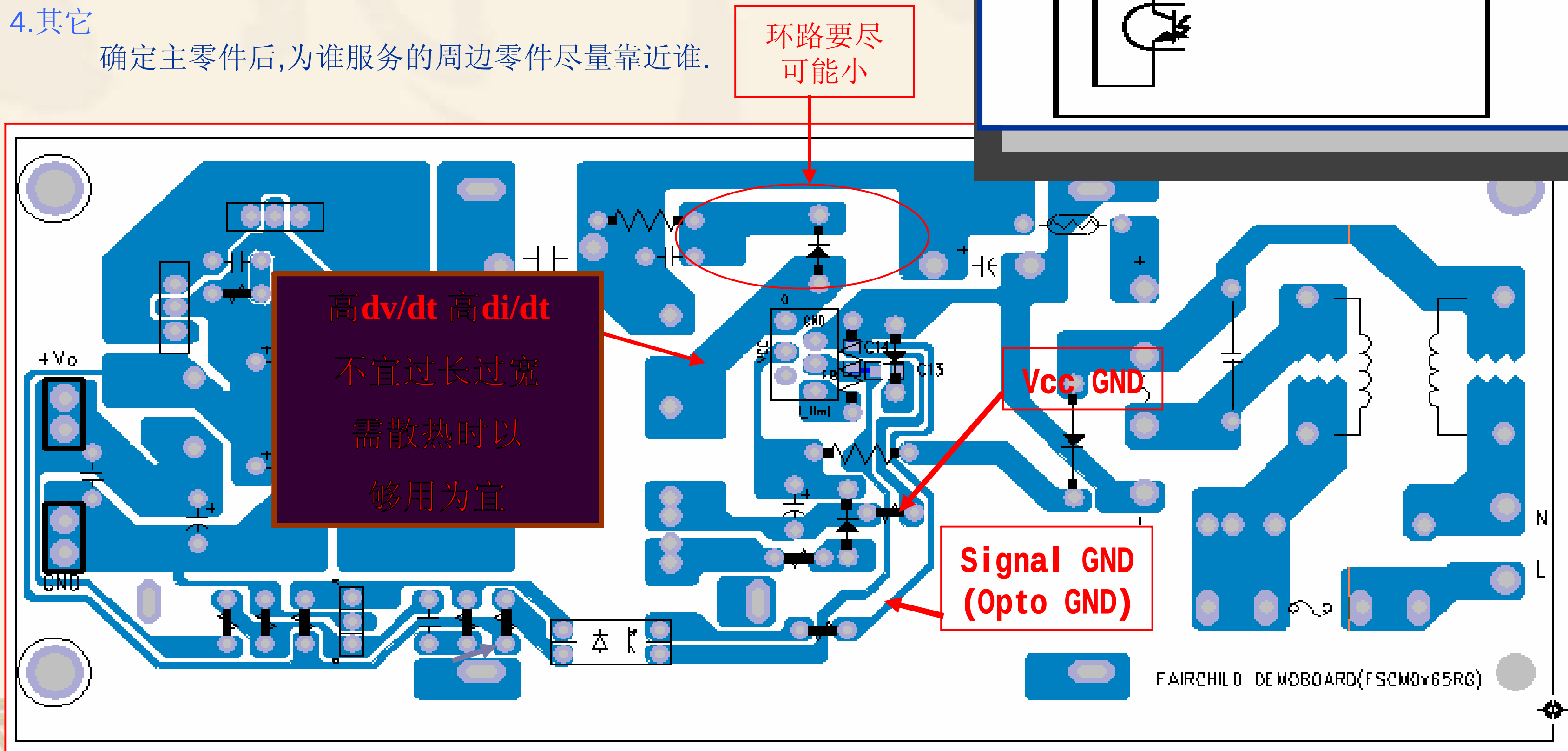
3.信号环路(特别是反馈信号)

信号地独立布线,尽可能与功率地分离. 光耦地，Vcc地，Y电容地分开,反馈脚电容靠近IC.

4.其它

确定主零件后,为谁服务的周边零件尽量靠近谁.





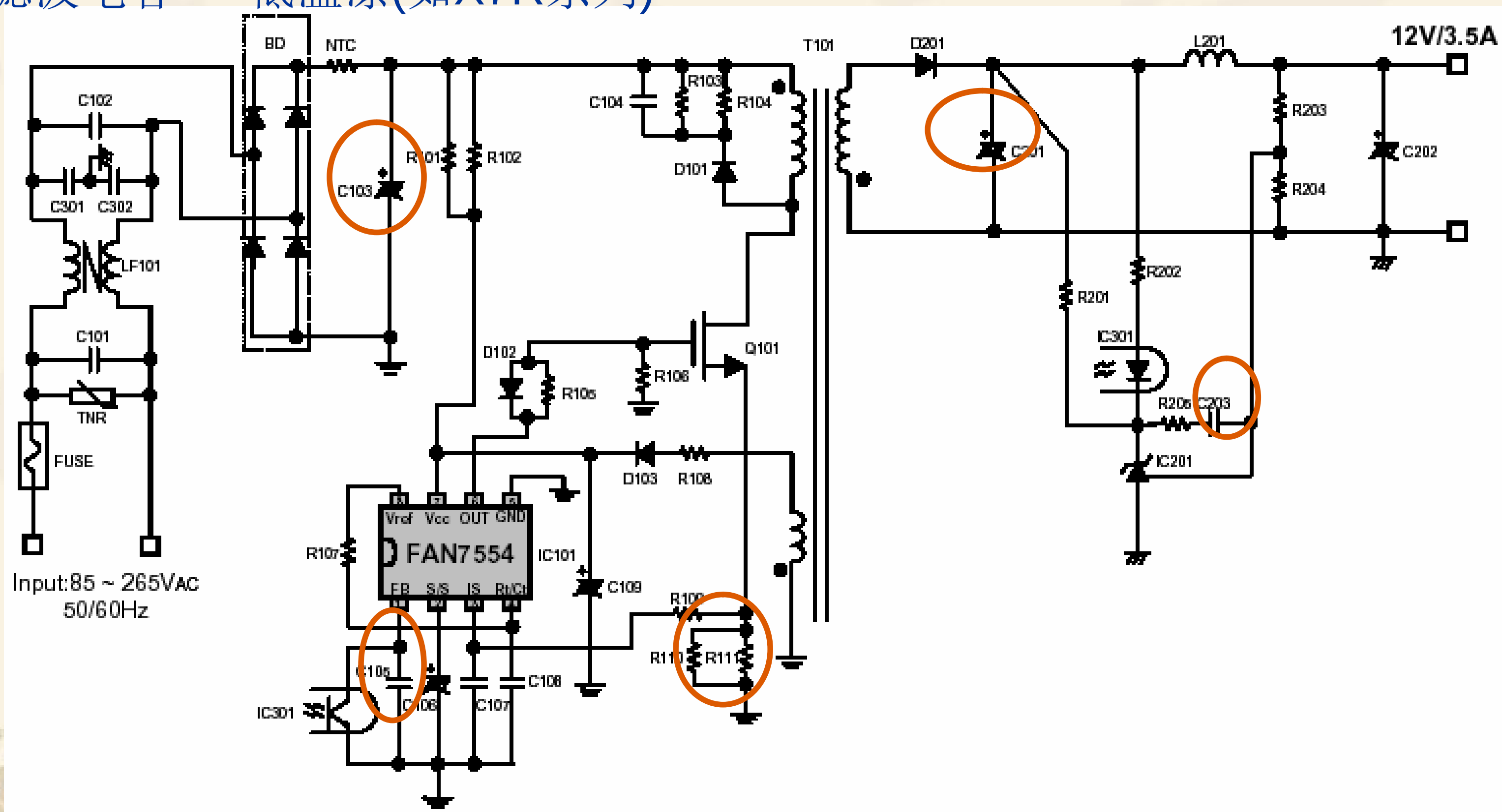
C,开关电源设计的一些考虑--零件选择注意点

1.电容

高压大电容¡　(1-3)uF/W,低等效串联阻抗(ESR)
输出滤波电容 --- 低等效串联阻抗(ESR)
反馈补偿电容 --- 低温漂(如X7R系列)
反馈滤波电容 --- 低温漂(如X7R系列)
¡

2.电阻

电感电流采样电阻--- 无感电阻
¡



C, Transformer Core Saturation 磁芯饱和

- 当使用FPS时还要注意验证变压器的饱和问题.
- 习惯的,
  - 磁心 Core is EE1616 (Ae=20mm²);
  - 初级电感 Lm is 2.2 mH;
  - 初级圈数primary turn number is 125 T
  - used IC is FSD210B
    - 275 mA ≤ I_{LIM} ≤ 365 mA

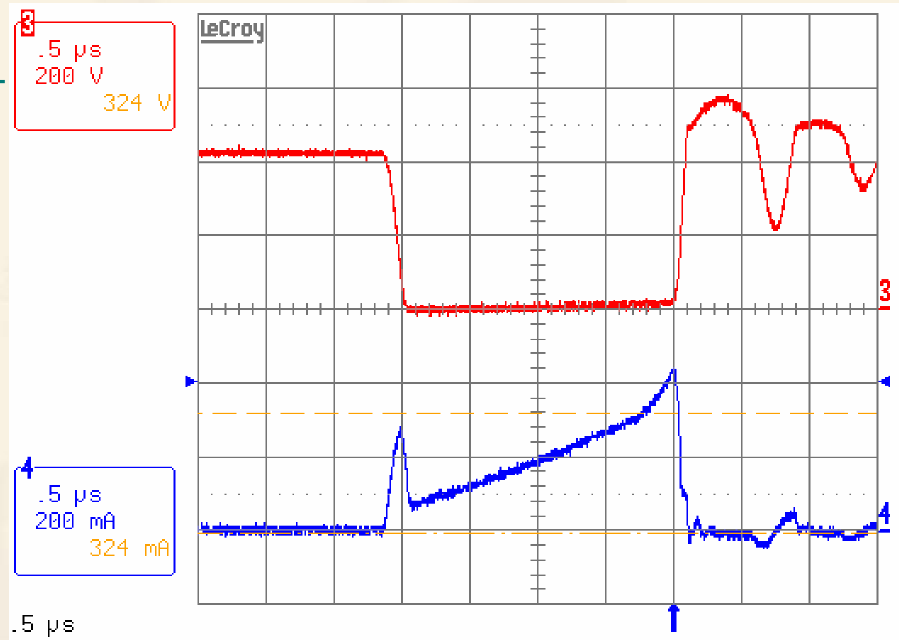
$$I_{Sat} = \frac{N_P \times B_{Sat} \times A_e}{L_m}$$

$$= \frac{125 \times 0.3 \times 20 \times 10^{-6}}{2.2 \times 10^{-3}}$$

$$= 340mA$$

≤ 365 mA

dangerous



C, Transformer Core Saturation 磁芯饱和

- Keep this equation in your mind记住这个公式:

$$I_{Sat} = \frac{N_P \times B_{Sat} \times A_e}{L_m}$$

  - I_{Sat} : 变压器 饱和电流
  - N_P : 初级匝数
  - B_{Sat} : 饱和磁感应强度
  - (generally, B_{Sat} = 0.3 T at T = 100 ¡C)
  - A_e : 有效磁面积
  - (generally, EE1616 Ae = 20¡ 10^{-6} m^2)
  - L_m : 变压器初级电感
- 如果Isat 比IC的限流点低,
- Increase Np; **增加匝数**
- Decrease Lm. **减小初级感量**
- 加上限流脚的电阻或减小其感量(影响输出功率)

C,开机问题 Startup issue

1.症状Symptom

FPS在满载或峰值负载时不能开机
输入90Vac~264Vac 低压倍压

FPS can not startup at full/peak load.
Input:90Vac~264Vac with doubler.

2.原因Root cause

开机时IC过载保护被触发
如果反馈脚电压到达6.5V 电源会进入过载保护状态，现在在光耦起作用之前，反馈脚已达此电压，过载保护被触发。

The device enters OLP mode at startup.
If the Vfb reaches 6.5V the device will enter OLP mode.Now the Vfb reaches 4.5+/-0.5V before the photo-coupler is under controled. The protection circuit is triggered and the device is in OLP mode.

开机问题Startup issue

解决方法Solution

方法Solution A) -----------增加反馈脚电容 Increase the Cfb.

优点：不用更改线路板，只需更改反馈电容值

缺点：输出电压纹波稍微增加

这种方法是增加反馈电压从0到6.5V的时间来达到开机目的。但限制了环路脉宽输出纹波会增加

--Advantage: Need not change PCB layout,only change the value of the Cfb.

--Disadvantage:The ripple voltage will increase a little.

This way is to increase the time of the Vfb reach 6.5V from 0V. But it will limit the bandwidth, and the ripple voltage will increase a little in burst mode(standby).

开机问题Startup issue

方法Solution B)--------加强外部软启动，使光耦在反馈电压到达6.5伏之前作用

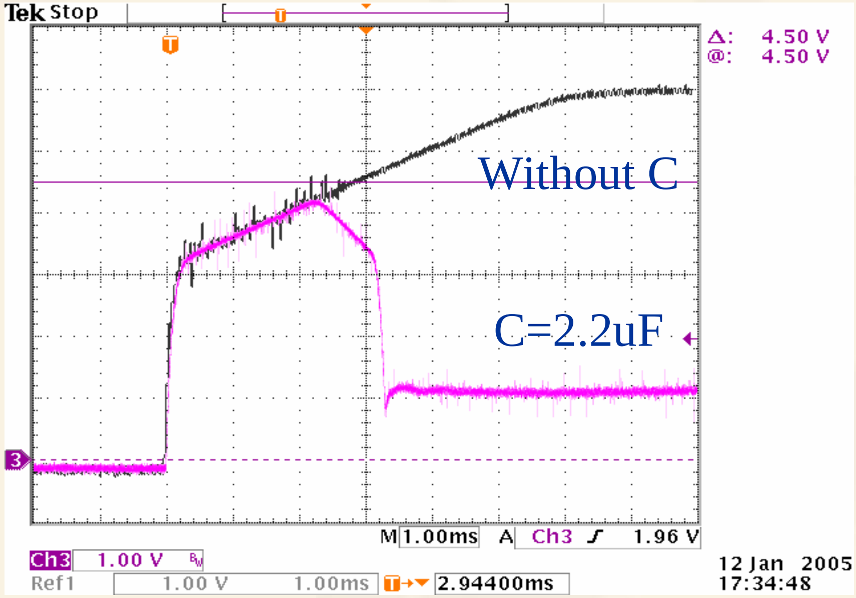
Enhance the external soft start, make the photocoupler under controlled before Vfb reaches 4V .

--Advantage: The output ripple and dynamic response almost no change .

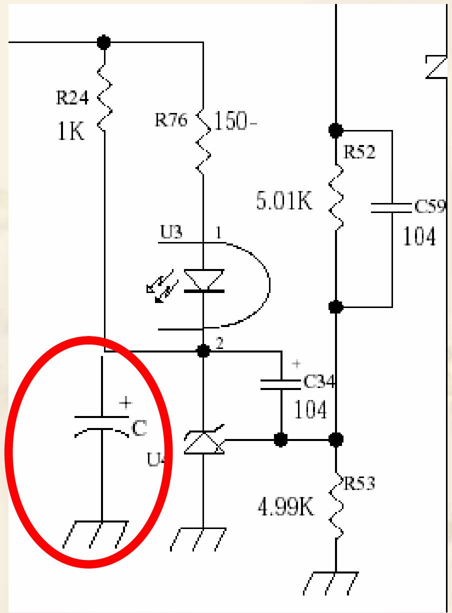
--Disadvantage:Need to adding position for the capacitor.

Add a capacitor cross the Pin_K and Pin_A of the 431.The value may be 2.2~4.7uF.

Test condition:Cfb=103



Vfb Io=2A



开机问题Startup issue

方法Solution C)--------增加1个电容＆1个稳压管－最好

Add a capacitor and a zener--- Best way

优点：只影响反馈电压升高到6.5V的时间，不影响工作时的环路响应

缺点：线路板修改

--Advantage: It can delay Vfb to reach 6.5V only in OLP, will not effect system response and loop gain in normal operation and standby mode.

--Disadvantage:Need to modify PCB layout.

The way is to add a cap and a zener cross feedback Pin and the GND. The fig below shows the connection. This solution is recommended by our application note AN4141.

This solution is better than solution A.

By setting the zener breakdown voltage (Vz) slightly higher than 3V(must below 4V), the additional delay capacitor (Cz) is isolated from the feedback circuit in normal operation. When the feedback voltage exceeds the zener breakdown voltage (Vz),Cz together with CB determine the shutdown time.

Test condition:Cfb(C11)=103

Cz:333

Vz:3.3V